Self-Aligned Carbon Nanotube Thin-Film-Transistors on Flexible Substrates with Novel Source-Drain Contact and Multi-layer Metal Interconnection

Daniel T. Pham, Harish Subbaraman, Maggie Yihong Chen, Senior Member, IEEE, Xiaochuan Xu, and Ray T. Chen, Fellow, IEEE

Abstract—This paper presents the development and characterization of self-aligned carbon nanotube thin-film transistors (CNT-TFT) on flexible substrates. The channel consisting of dense, aligned, 99% pure semiconducting single-walled carbon nanotube (SWCNT) are deposited using dip-coat technique on sacrificial substrate and then transferred on the device substrate. The source, drain and gate structures are formed by ink-jet printing technique. A novel source-drain contact formation using wet droplet of silver ink prior to CNT thin-film application has been developed to enhance source-drain contact with the CNT channel. Bending test data on CNT-TFT test structures show minimal change (less than 10%) in their performance. Moreover, a special multi-layer metal interconnection technology is demonstrated for flexible electronics applications. Bending test data on via test structure show change in resistance by less than 5%.

Index Terms—carbon nanotube, thin-film transistor, flexible electronics, single-walled carbon nanotube, dip-coat technique.

I. INTRODUCTION

Ink-jet printing technique is a simple and cost effective method to produce electronics. It is an attractive process for flexible electronics due to its non-contact and additive deposition technique. The technique does not require sacrificial resist or liftoff layers but rather deposits materials only where needed. Soluble organic materials have been used as the channel material for several state-of-the-art flexible electronics [1,2]. However, the carrier mobility of organic semiconductor polymers is less than $1.5 \text{cm}^2/\text{Vs}$ [3,4]. This limits the organic polymer TFT’s operating speed to only a few KHz. On the other hand, carbon nanotube (CNT) based thin-film transistors have seen tremendous improvements over the last five years due to their excellent mobility characteristics [5,6]. Extremely high mobility of 100,000$\text{cm}^2/\text{Vs}$ of individual CNTs has been reported [6]. CNT TFT-based devices on flexible substrates have achieved high field mobilities using ultrapure electronics-grade CNT solutions [7,8] by ink-jet printing technique. CNT in solution can be printed; however, it often clogs up the nozzles. Other techniques such as dielectrophoresis [9], spin-coat [10], and spray [11] to form CNT thin-film transistor have been demonstrated. These techniques yield a random network of CNTs on the substrate. However, in order to retain the attractive properties of individual CNTs, it is desirable to have densely packed, perfectly aligned, horizontal arrays of CNTs thin-film as the channel of the TFT device. Most of the reported aligned CNT thin films are deposited on silicon or quartz substrates via the chemical vapor deposition (CVD) technique [12,13,14]. This deposition technique is unsuitable for flexible substrates because of the high deposition temperature.

In this work, we fabricate CNT-TFT using a combination of ink-jet printing and stamping (for CNT layer) techniques, with self-aligned-CNT channel, novel source-drain contact, and multi-layer metal interconnect.

II. FABRICATION PROCESS

A. Ink-jet printing

Ink-jet printing is performed using the Dimatix DMP 2800 (Dimatix-Fujifilm Inc., Santa Clara, USA), which uses piezoelectric printing cartridge (DMC-11610). The ink droplet dispensed from the ink cartridge has a nominal volume of 10pL. One or more nozzles can be used for the printing. For small TFT structure used in this work, only one nozzle is used. For other large structures such as probing pads, via pads, etc., up to 16 nozzles are used. The temperature of the platen and cartridge is set at room temperature. Silver ink from Cabot Corporation (CCI-300) is used for the source, drain and gate electrode printing. Spin-on glass is used as dielectric ink. Customized waveform patterns in the printer are used to print silver and dielectric inks.
B. Carbon Nanotube deposition

Using the dip-coat technique, CNTs can be self-aligned on the substrate [18]. Dip-coating technique has been widely used to deposit particles uniformly on different surfaces [15,16,17]. The main driving force for the convective transfer of CNTs is evaporation of the solvent. As the solvent starts to evaporate, the convection force transfers the CNTs to the contact line (solid-vapor-liquid interface), thus depositing CNTs on the substrate [15,16]. Depending on the concentration, particle size, and drying speed, single or multiple layers can be obtained. We observe that stripes of CNTs thin film are obtained at high drying speeds. This occurs when the capillary force, which pulls the liquid inwards, builds up and exceeds the surface tension of the liquid. When this happens, a new contact line is formed as shown in Figure 1. In this work, 99% pure semiconducting single walled carbon nanotubes in surfactant solvent from Nanointegris, Inc is used (S10-671, 0.1mg in 10mL aqueous solution) for the dip-coat technique to deposit CNTs on a silicon substrate (acting as sacrificial substrate). The surfactants keep the CNTs from bundling with each other, which assists in the self-alignment process. Figure 1a shows the SEM image of stripes of CNT, with the surfactant, formed using our process. Rinsing the substrate in 2-propanol causes the surfactants to dissolve away, thus leaving CNT on the substrate as shown in Figure 1b. Further suspending the substrate in 2-propanol for 15 minutes entirely removes the surfactants and exposes the CNTs as shown in Figure 1c. Note that some amount of CNT is also lost during this process. In this process, the stripe width can be controlled by temperature (evaporation speed), solvent properties, particle density, and substrate surface roughness.

C. Process Integration

Both top gate and bottom gate integration approaches are studied. Table 1 show the comparison of both integration schemes.

<table>
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<tr>
<th>Integration</th>
<th>Advantage</th>
<th>Disadvantage</th>
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<tr>
<td>Top gate</td>
<td>♦ CNT channel deposited first ♦ Dielectric &amp; gate electrode cover the channel (passivating the channel) ♦ CNT channel has good contact with the annealed source-drain metal printed on top of the channel</td>
<td>♦ Dielectric material diffuses between CNTs and separate them ♦ High thermal budget applied on the CNT channel.</td>
</tr>
<tr>
<td>Bottom gate</td>
<td>♦ CNT channel deposited last – No interaction with dielectric and gate materials ♦ Low thermal budget for CNT channel</td>
<td>♦ CNT channel has bad contact with source-drain areas (solution identified in this paper) ♦ No passivation – exposed to air (solution identified in the paper)</td>
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Due to its attractive advantages of low thermal budget and least interaction with dielectric and gate materials, bottom gate integration approach is utilized in this work. In order to overcome the disadvantages, novel solutions have been addressed in this paper. The schematic of the bottom gate integration process flow is shown in Figure 2. A Kapton Polyimide substrate with a thickness of 127µm is used. The gate electrode is first printed on the Kapton film using silver ink, followed by thermal annealing at 160°C for 10 minutes. Spin-on-glass is used as the dielectric material, which is also printed. The source and drain regions are printed using the same silver ink as used for gate electrode and under the same annealing conditions. The device channel length is 100µm and width is 300µm. For the small structure, only one nozzle is used during the printing in order to maintain resolution.

![Fig. 1. (a) SEM image showing the stripe of CNT with surfactant. (b) Zoom-in SEM image of self-aligned CNT thin film with surfactant, (c) SEM image of self-aligned CNT thin-film after suspended in alcohol bath.](image-url)
The 99% pure semiconducting CNT from Nanointegris, Inc is deposited on the silicon substrate (as a sacrificial substrate) using dip-coating technique, as discussed in section II b. In order to transfer the CNT thin-film on to the flexible Kapton polyimide substrate, another special Kapton substrate (25µm thick), with adhesion coating on one side, is used to lift the self-aligned CNT thin-film from the silicon substrate and lay it on top of the first substrate over the printed channel region. The Kapton with adhesive is left on the device in order to protect the CNT channel, thus acting like a passivation layer.

Prior to bonding these two layers, a novel technique to enhance the contact between CNT and source-drain areas is developed. In this technique, droplets of silver ink are printed on the source and drain areas on the first substrate as shown in Figure 3. These wet silver ink droplets allow the silver liquid to “wet” the CNT thin-film area and enable good contact with the printed source and drain contact. In order to bond the two substrates, the device is left under pressure on a heat chuck surface at 100°C for 30 minutes to enhance the bonding of the second Kapton substrate to the first substrate and eliminate any air pockets. Upon bonding and annealing, the source-drain contact junction is formed into the CNT thin-film, thus providing a good contact with the entire thin film. Without using the wet silver droplets to enhance the contact, the ON current is very low ranging from a few nano to a few micro-amps.

III. CHARACTERIZATION OF THE SELF-ALIGNED CNT-TFT

Figures 4(a) and (b) show the measured I-V characteristics (I_D versus V_DS) of the self-aligned CNT-TFT as a function of different gate voltages (V_G). The transistor I-V characteristics are measured using precision semiconductor parameter analyzer (Agilent 4156C). At a gate voltage of 0V gate, the device does not show pinch-off, most likely due to a small number of metallic nanotubes in the channel. At V_G=-3V and source-drain voltage (V_DS) of -1V, high drive current of 0.371mA is obtained, which is in good agreement with the high density and self-aligned nature of CNTs on the device channel. As mentioned in Engel et al. [18], CNT-TFT can have I_on/I_off ratio as high as 10^5; however, any improvement for the on-state current will degrade the I_on/I_off Ratio due to the increased number of metallic pathways between source and drain. In this experiment, we observe the I_on/I_off ratio of around 20. Further optimizations such as using electrical burning off technique to eliminate metallic pathways will be reported in a future publication.

![Graph](image-url)

**Fig. 2.** Bottom gate integration with novel source-drain and CNT contact.

**Fig. 3.** Wet silver droplets on source-drain areas before bonding with CNT thin-film.
Bending test is performed on the device. Figure 5 shows the picture of bending test structures. Two different test structures are formed to evaluate the vertical and horizontal orientations of the transistor. Three different radii of curvature, 4.5mm, 3mm and 1.5mm, are used in this evaluation. Forward and backward bending tests are conducted as described in Figure 5.

![Bending test structure](image)

**Fig. 5.** a) Bending test structure for vertical and horizontal devices, b) Device under backward bending test at 1.5mm radius of curvature.

Figure 6 show the normalized drain current ($I_{D,\text{test}} / I_{D,\text{original}}$) plotted against radius of curvature for the vertical test structure. In forward bending, lower drain current is observed, with up to 10% change, while no significant drain current difference is observed in backward bending case. Larger current change for vertical test structure can be attributed to the 300μm channel width of the testing device subjected to the bending direction. Since the CNTs are captured by the thinner Kapton film that is bonded onto the thick Kapton substrate, forward bending may cause movement to the thin kapton film move away from substrate, while in backward bending, it causes the thin Kapton film to press against the substrate.

![Normalized Drain Current](image)

**Fig. 6.** Bending test data for vertical test structure.

Figure 7 shows drain current bending test data for horizontal test structure. Smaller change in drain current is observed (less than 6%). For the horizontal test structure, 100μm channel length of the device is subjected to the bending direction. In the forward bending case, shorter channel length causes a small increase in current, and in backward bending case, “stretched” channel length reduces the current (even though the thin top layer Kapton is pressed against the substrate).

![Normalized Drain Current](image)

**Fig. 7.** Bending test data for horizontal test structure.

### IV. Multi-Layer Metal Interconnect

In order to develop full systems such as large area printed phased array antennas utilizing CNT-TFTs as RF amplifiers, the signal layout scheme will be extremely complicated and prohibitive if performed in one dimension (i.e. all interconnection lines, other components and CNT-TFTs printed in the same layer). Similar to silicon semiconductor devices, such complex flexible electronics also require multiple layers and interconnections for its circuits. Especially, CNT-TFTs will all be formed in one layer and the signals will be routed to and from these FET to all other components through various stacked layers. Therefore, considering such a requirement for futuristic applications in mind, in this paper, we also report a technique to form multiple layers metal interconnection on flexible substrates and show multilayer interconnection to the fabricated CNT-TFT device. After forming the CNT-TFT device layer, a special Kapton substrate
(25 µm thick), with adhesive coated on one side, is used to glue on top of the first substrate. Contact vias are formed prior to attaching in order to obtain metal contacts with the gate contact pads on the bottom substrate. The via diameter used in the work is 1 mm (available cylinder blade to cut the via with that size). The adhesion of this layer is critical since any voids between layers will cause the liquid silver ink to spread between these layers due to the capillary effect. An annealing process is used after bonding these layers together by pressing against a heat chuck at 100°C for 30 minutes. Then, the silver ink is printed on top of the top Kapton layer for the metal interconnection lines on top substrate. The printed silver ink penetrates through the vias to contact the gates on the first layer. Following this, another anneal process is performed in order to evaporate the solvent in the silver ink and form a good Ohmic contact. Figure 8 shows the schematic of multi-layer metal interconnect integration for flexible electronics performed in this work.

In order to evaluate the type of contact formed, we form a test structure as shown in Figure 9. From the resistance measurements, we observe no resistance difference between the two contact pads with and without interconnect via. Figure 9a and 9b show via development test structure, pre- and post silver ink printing on second Kapton layer. To protect the metal contact line and via, the Kapton substrate with adhesive coating is bonded on top (Figure 9c). This layer acts as a passivation or protection layer for the circuit and protects it from environment as well as its mechanical strength.

![Diagram](image_url)

Fig. 8. Multi-layer metal interconnect integration scheme.

Figure 10 shows the bending test for via test structure. Lower resistance value is observed when bending to small radius of curvature. It indicates that the via is not completely filled with silver ink. Silver thickness on flat surface is measured to be around 0.4 µm. The via diameter is 1 mm, and the metal interconnect line is 300 µm wide. In forward bending, the via might squeeze the silver particles together causing lower resistance data. While in backward bending, the top passivation Kapton layer applies pressure to the silver particles in the via.

![Bending Test Data](image_url)

Fig. 10. Bending test data for via test structure.

V. SUMMARY

In this paper, we demonstrate a self-aligned CNT-TFT using 99% pure semiconducting nanotube on flexible Kapton substrate. A novel source-drain contact is developed to enhance the contact with CNT channel. Bending test data show minimal changes (less than 10%) in their performance. Multiple layer interconnect integration is also demonstrated on a flexible substrate circuit. These developments lift strong constraints for flexible electronics, providing an open route for realistic applications using self-aligned CNT-TFT and multiple layer interconnection for flexible electronics technology.
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REFERENCES


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He received the B. E. degree in Electronics and Communication Engineering from Chaitanya Bharathi Institute of Technology, Hyderabad, India, in 2004, and the M.S and Ph. D degrees in Electrical Engineering from the University of Texas at Austin in 2006 and 2009 respectively. With a strong background in RF photonics and X-band Phase Array Antennas, Dr. Subbaraman has been working on true-time-delay feed networks for phased array antennas and carbon nanotube based thin-film transistors for the last 4 years. Throughout these years, he has laid a solid foundation in both theory and experimental skills. He has served as principal investigator for projects from National Aeronautics and Space Administration (NASA), Air Force Office of Scientific Research (AFOSR), and NAVY. Dr. Subbaraman has over 15 publications in refereed journals and conferences.

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holds the Cullen Trust for Higher Education endowed professorship at UT Austin and the director of nanophotonics and optical interconnect research lab within the microelectronics research center. He is also the director of a newly formed AFOSR Multi-disciplinary Research Initiative (MURI) Center for Silicon Nanomembrane involving faculty from Stanford, UIUC, Rutgers and UT Austin. He received his BS degree in Physics from National Tsing-Hua University in 1980 in Taiwan and his MS degree in physics in 1983 and his PhD degree in Electrical Engineering in 1988, both from the University of California. He joined UT Austin as a faculty to start optical interconnect research program in the ECE Department in 1992. Prior to his UT’s professorship, Chen was working as a research scientist, manager and director of the Department of Electrooptic Engineering in Physical Optics Corporation in Torrance, California from 1988 to 1992. Chen also served as the CTO/founder and chairman of the board of Radiant Research from 2000 to 2001 where he raised 18 million dollars A-Round funding to commercialize polymer-based photonic devices involving over 20 patents, which was acquired by Finisar in silicon valley(NASDAQ: FNSR). He also serves as the founder and Chairman of the board of Omega Optics Inc. since its initiation in 2001. Over $5 million dollars of research funds were raised for Omega Optics. His research work has been awarded with 99 research grants and contracts from such sponsors as DOD, NSF, DOE, NASA, the State of Texas, and private industry. The research topics are focused on three main subjects: 1. Nano-photonic passive and active devices for optical phased array and interconnect applications. 2. Thin film guided-wave optical interconnection and packaging for 2D and 3D laser beam routing and steering, and 3. True time delay (TDD) wide band phased array antenna (PAA). Experiences garnered through these programs in polymeric material processing and device integration are pivotal elements for the research work conducted by Chen’s group.

Chen’s group at UT Austin has reported its research findings in more than 540 published papers including over 60 invited papers. He holds 20 issued patents. He has chaired or been a program-committee member for more than 100 domestic and international conferences organized by IEEE, SPIE (The International Society of Optical Engineering), OSA, and PSC. He has served as an editor or co-editor for eighteen conference proceedings. Chen has also served as a consultant for various federal agencies and private companies and delivered numerous invited talks to professional societies. Dr. Chen is a Fellow of IEEE, OSA and SPIE. He was the recipient 1987 UC Regent’s dissertation fellowship and of 1999 UT Engineering Foundation Faculty Award for his contributions in research, teaching and services. We is also the recipient of 2008 IEEE teaching award. Back to his undergraduate years in National Tsing-Hua University, he led a university debate team in 1979 which received the national championship of national debate contest in Taiwan. There are 33 students received the EE PhD degree in Chen’s research group at UT Austin.